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TOWNSEND and TOWNSEND and CREW LLP

By: Olivia Elzinga

PATENT

Attorney Docket No.: 018757-004600US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chun-Mai Liu et al.

Application No.: 09/827,056

Filed: April 3, 2001

For: METHOD OF FABRICATING HIGH-COUPLING RATIO SPLIT GATE FLASH MEMORY CELL ARRAY

Examiner: Thomas J. Magee

Art Unit: 2811

APPELLANT'S BRIEF UNDER 37 CFR 1.192

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicants appeal the final rejection of claims 1–14 and 16 in the above-captioned patent application. The claims on appeal have been finally rejected pursuant to MPEP 706.07(a). Accordingly, this appeal is proper and is filed in triplicate.

I. REAL PARTY IN INTEREST:

The real party of interest of the above-identified application is Winbond Electronics Corporation, a Taiwan company having its principal place of business at No. 4, Creation Road III, Science-Based Industrial Park, Hsinchu, Taiwan, ROC. The assignment is recorded in the U.S. Patent and Trademark Office on at Reel/Frame 011685/0699.

II. RELATED APPEALS AND INTERFERENCES:

There are no appeals or interferences related to the present appeal.

III. STATUS OF CLAIMS:

Claims 1–14 and 16 are pending and are the subject of this appeal. Claims 1 and 14 are objected to for certain informalities in the Final Office Action dated 10/20/2003. The Examiner stated that ' ... In Claim 1, "said predefined areas having been implanted with said ions," is redundant. Similarly, in Claim 14, the phrase, " ... said common region having a portion that has been implanted with said first ions," is repetitive. Corrections are required.' Applicants respectfully disagree.

All pending claims 1 – 14 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lin et al., (US 6,355,527) in view of what the Examiner indicated was admitted prior art in the same Final Office Action mailed October 20, 2003. Applicants also disagree to the Examiner's rejection.

IV. STATUS OF AMENDMENTS:

There are no amendments filed after the final rejection. In accordance with 37 C.F.R. 1.192 (c) (9), a copy of the claims involved in the appeal is contained in the Appendix attached hereto.

V. SUMMARY OF THE INVENTION:

The present invention relates to a method of fabricating a split gate flash memory device, including cells having an increased coupling ratio thereby reducing the time and voltage required to program each cell. More particularly, the invention also includes threshold voltages adjustment by implanting ions into portions of the substrate defined by the floating gate regions, , to allow for precise threshold voltage control. Details of the claimed method are provided below.

A preferred embodiment of the present invention provides a process of fabricating a flash memory device including an array of split gate cells. The method includes providing a silicon substrate having a top surface and forming a common source region in an area of the top surface for each pair of said cells [Page 5, line 30 to page 6, line 2, and Fig. 2A]. The process requires a certain process sequence for selected steps in the manner claimed. Preferably, the method implants ions into predefined areas of each common source region [Page 6, lines 3 – 15, and Fig. 2B] and then forms floating gates associated with the cells. That is, the formation of the floating gates occurs after implantation of ions into predetermined areas. Each floating gate has a substantial portion thereof overlying one of the predefined areas, which have already been implanted with ions from the previous step of implantation [Page 6, line 16 to page 8, line 3, Figs 2C-2E. The method then forms select gates, each having a first extremity extending over at least a portion of one of the floating gates [Page 8, lines 4-14, Figs. 2F and 2G]. The method also

forms drain regions associated with the cells. Each of the drain regions is positioned proximate a second extremity of one of the select gates [Page 8, lines 15-21, Fig. 2H]. The present process leads to certain benefits associated with the coupling ratio and threshold voltage as will be described in further detail below.

An aspect of the invention relates to a method of forming the floating gates of the flash memory device [Page 6, line 16 to page 8, line 3, Figs 2C-2E]. The method includes forming a tunneling oxide layer over the top surface area of the substrate, depositing a first polysilicon layer over the tunneling oxide layer, and depositing a nitride masking layer over the first polysilicon layer [Page 6, lines 16-24, Fig. 2C]. The process also includes patterning and etching the nitride masking layer to expose first and second portions of the first polysilicon layer, and the exposed first and second portions substantially define first and second floating gate regions [Page 6, lines 24-25, Fig. 2C]. Here the patterning process is used to determine the overlap between the floating gates and the source region [Fig. 2C]. A threshold implantation step occurs after the patterning process.

Specifically, the method then implants ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of the common source region, in order to adjust the threshold voltage of the flash memory device [Page 6, lines 26-31]. This implanting step allows precise control of threshold implant under the floating gate. The method continues with forming a floating gate oxide layer over the first and second exposed portions of the first polysilicon layer [Page 7, lines 5-11, Fig. 2D]. After removing the nitride masking layer, the method then etches the first polysilicon layer and the tunneling oxide layer using the floating gate oxide layer as a mask. This method leaves remaining portions of the first polysilicon layer and the tunneling oxide layer disposed beneath said floating gate oxide layer, and exposes a portion of the substrate. The remaining portions of the first polysilicon layer form first and second floating gates associated with each cell. These floating gates have side walls and a portion which overlies a portion of the common source region, thereby providing a high coupling ration for the associated cell [Page 7, lines 13-18, Figs. 2D and 2E]. As described earlier, determines the extent of the overlap and, therefore, the coupling ratio [Fig. 2C-2E].

Using the specific process of the present invention, certain benefits are achieved over conventional techniques. The present process is easy to use and avoids certain processing difficulties of the prior art. Additionally, the step of implanting ions into each of the predefined first and second floating gate regions adjusts the channel threshold voltage to provide precise threshold voltages [Page 3, lines 27 – 31]. The step of forming the floating gates after implanting the source region allows the floating gate patterning step to determine the desired overlap between the floating gate and the source region, and, as a result, provides a high coupling ratio for the associated flash cells. In contrast, in conventional devices the coupling between source and floating is limited by the side diffusion of the ions implanted after the floating gate formation [Page 2, line 24 to page 3, line 26]. The high coupling ratio allows for improved programming of the present flash memory device and reduces the time and voltage

required to program each cell. These and other benefits will be described throughout the present appeal and more particularly below.

VI. ISSUES

The following issues are presented:

1. Whether the Examiner properly objected to claims 1 and 14.
2. Whether claims 1 –1 4 and 16 were properly rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of what the Examiner considers admitted prior art.

VII. GROUPING OF THE CLAIMS:

In the present case, the rejected claims do not all stand or fall together. Applicants submit that certain claims present distinct issues concerning patentability. For purposes of preserving these distinct issues, Applicants group the claims as follows.

Group 1: Claim 1, which stands or falls by itself.

Group 2: Claim 2, which stands or falls by itself.

Group 3: Claim 3, which stands or falls by itself.

Group 4: Claim 4, which stands or falls by itself.

Group 5: Claims 5 and 9, which stand or fall together.

Claim 6: Claim 6, which stands or falls by itself.

Group 7: Claim 7, which stands or falls by itself.

Group 8: Claim 8, which stands or falls by itself.

Group 9: Claim 10, which stands or falls by itself.

Group 10. Claim 11, which stands or falls by itself.

Group 11: Claims 12 and 13, which stand or fall together.

Group 12: Claim 14, which stands or falls by itself.

Group 13: Claim 16, which stands or falls by itself.

VIII. ARGUMENTS:

Because all the claims do not stand or fall together, Applicants present arguments for each claim group later in this brief. Before specifically discussing the Examiner's rejection as applied to each of the claim groups, Applicants first address the Examiner's basis for maintaining the rejection which was applied to all pending claims.

Improper Basis For Rejections

The Examiner has not appreciated that the invention of claims 1 and 14 require a certain chronology of steps. In the Final Office Action mailed October 20, 2003, the Examiner summarized the grounds for maintaining the rejection of claims 1 – 14 and 16 under 35 U.S.C. 103(a) in paragraph 14 on pages 9 and 10, as follows:

> "With regard to Independent Claims 1 and 14, Examiner must again reiterate that he can only interpret language posed in limitations of claims and currently, Lin et al. discloses those tenets recited in the claims of the instant application of Applicant. *There is no chronology of process steps disclosed in the reference or recited in the claims of the instant application.* Therefore, arguments appear moot." [Emphasis Added.]

Applicants respectfully submit that the claims 1 and 14 are patentable over the cited references. As noted earlier and further emphasized herein, claims 1 and 14 recite a certain sequence of steps requiring a chronology, which the Examiner has not appreciated. Using claim 1 as an example, it recites, *inter alia,*

> "*forming a common source region* in an area of said top surface for each pair of said cells;
>
> *implanting ions into predefined areas of each said common source region;*
>
> *forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions; ...*"

Since the floating gate is formed to overlie the predefined area, and the predefined area "has been implanted with said ions", it is clear that ion implantation into the common source region precedes the floating gate formation, such that a substantial portion of the floating gates overlies the implanted common source region in the substrate that has been implanted with the ions. Here, forming the floating gates occurs after the predefined area has already been implanted with ions, so that a substantial portion of the floating gate is formed to overlie the implanted common source region.

Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. In contrast, Lin et al. used a completely different process sequence. Column 6 lines 26 – 28 of Lin et al. stated, "source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." Further, Claim 1of Lin et al. (US 6,355,527) recites, inter alia,

> " ... etching said first polysilicon layer to form said floating gate using said regions of poly-oxide as a hard mask; **then**
>
> forming a second photoresist layer over said substrate and patterning to define source region; **then**
>
> performing ion implantation through openings in said second photoresist layer to form source region, ...; **then ...**"

The Examiner is mistaken in stating that: "no chronology of process steps disclosed in the reference or recited in the claims of the instant application." (Paragraph 14, Response to Arguments in the 10/20/2003 Office Action) As noted above, Lin et al. discloses the sequences of etching the first polysilicon layer, then forming a second photoresist, and then performing ion implantation, which are not the inventions of claims 1 and 14. Accordingly, claims 1 and 14 are patentable over Lin et al.

The Examiner also misunderstands how the "coupling ratio" is increased by Lin et al. and the invention of claims 1 and 14. The Examiner stated,

> " The lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling."

The Examiner further stated,

> "Applicant has apparently misread in reference, since the coupling ratio is due to the Distance source extends beneath gate, as claimed in the reference and also recited in the instant application."

Applicants note that, since the device in Lin et al. is formed with source implant after the floating gate formation, the coupling between source and floating gate is provided by lateral diffusion of source beneath gate. This side diffusion is limited, because the maximum allowable diffusion depth of the common source region is limited (See, specification of the instant invention, page 4 lines 23 – 30). Under such limitation, Lin et al. sought to obtain higher coupling ratio by coupling the floating gate with an extra polysilicon line. Lin et al. stated, "The main feature of the invention, ... to form a poly line (165) continuous over the source region (125')..." (Col. 6, lines 51 – 58) and " ... the poly line provides an additional vertical wall area along the edges of the floating gates (140). The additional area shares the voltage levels imposed between source (125) and the floating gate (140),...by virtue of the increased sidewall coupling area between the source and the floating gate , the coupling ratio is also increased..." (Col. 6, lines 64 – Col. 7 ,

line3). In contrast, the invention of claims 1 and 14 recites a different method for achieving higher coupling ratio.

The high coupling ratio flash cell device of the present invention overcomes the side-diffusion coupling limitation by forming the implanted common source region first, and then forming the floating gates (See, specification of the instant invention, page 4 lines 23 – 30). In this case, the extent of overlap of the floating gate over the implanted common source region is determined by the patterning process (page 6, line 16 to page 7, line 18, and figs 2C – 2E), instead of side diffusion. This pont is further explained in the Applicants' specification, page 8, line 27 – page 9 line 2, "The device 200 provides cells having an increased source side coupling ratio relative to the prior art. The increased source side coupling ratio is due to the distance 202 the source region extends beneath the floating gate 124A, 124B being increase over the distance 46 the prior art source region 42 (Fig. 1) extends beneath floating gate 22, 24 (Fig. 1). This increases in the distance the source region 116 extends beneath the floating gate 124A. 124B is provided by the method of the present invention."

Accordingly, the invention as recited in Claim 1 and 14 of the instant application provides a method to increase the extent of the overlap between source and floating gate without increasing the lateral diffusion and the diffusion depth of the source, thus providing an increased coupling ratio. Lin et al. does not show or suggest these claimed features. Therefore, claims 1 and 14 are patentable over Lin et al.

Claim Objections

The Examiner objected to claims 1 and 14 in the Final Office Action mailed October 20, 2003,

"In Claim 1, the recitation, 'said predefined areas having been implanted with said ion,' is redundant. Similarly, in Claim 14, the phrase, '.... said common source region having a portion that has been implanted with said first ions,' is repetitive. Corrections are required."

Applicants note that the recitations were introduced in Applicants' 08/18/2003 amendment for the purpose of clarifying the chronology of the process sequence, in response to the 6/18/2003 Office Action But as discussed earlier, the Examiner still fails to appreciate the chronology and regarded these phrases redundant and repetitive. Applicants submit that with the amendment of the recitation, "said predefined areas having been implanted with said ion," in claim 1, it is now clear that the floating gate is formed after the common source region has been formed and has been implanted with the ions, because the floating gate has a substantial portion overlying the area which has been implanted with the ions. Similarly, in claim 14, the recitation, "'.... said common source region having a portion that has been implanted with said first ions," further clarifies that the floating gate is formed after the common source region has been formed and has been implanted with the ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed.

Therefore, claims 1 and 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Applicants request that the Examiner's objections to Claims 1 and 14 be removed.

Rejection of claims under § 103(a)

The Examiner rejected Claims 1 – 14 and 6 under 35 U.S.C. 103(a) as unpatentable over Lin et al. (US 6,355,527) in view of wht the Examiner considers admitted prior art. Applicants respectfully traverse the rejection of these claims.

To establish a *prima facie* case of obviousness under §103(a), each of three requirements must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine references or modify a reference. (MPEP § 2143.01.) Second, a reasonable expectation of success must exist that the proposed modification will work for the intended purpose. (MPEP § 2143.02.) Moreover, both of these requirements must "be found in the prior art, not in applicant's disclosure." (MPEP § 2142.) Third, the reference or references, taken alone or in combination, must disclose or suggest every element recited in the claims. (MPEP §2143.03.)

Because all the claims do not stand or fall together, Applicants will present argument for each claim groups.

Claim Group 1

The Examiner has maintained his rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI ERA: Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322). Here, the Examiner suggested that Lin et al. disclosed a method for forming split-gate flash memories with improved, increased coupling ratio and that Wolf, pp. 321 – 322, showed adjustment of channel threshold voltage using ion implantation. The Applicants disagree with the Examiner's argument.

In rejecting Claim 1, the Examiner stated in the 10/20/2003 Office Action,

> "Regarding Claim 1, Lin et al. clearly disclose a method for forming split-gate flash memories with improved, increased coupling ratio. A common source region is formed (125) (Figure 2G) in a silicon substrate. Source implantation is done using n-type implants (Col. 6 lines 42 – 45) and drains (120) implanted at opposite sides of the source (and within the vicinity (second extremity) of gate regions) (Figure 2G) using n-type implants (Col 7, lines 14 – 18). Floating gates (140) (Figure 2D) are formed, overlying areas of the common source region (Figure 2D) and extremities extending over the (first) part of the structure."

It appears that the Examiner ignored the chronology in Lin's disclosure, both in the specification and claims, which forms the floating gate before the source region implant, , as discussed earlier, Also as discussed earlier, Claim 1 of the instant invention clearly demonstrate a chronology. Claim 1 now recites floating gate formation after ion implantation into the common source region , such that a substantial portion of the floating gates overlies the implanted common source region in the substrate. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. Lin fails to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions." Wolf also failed to teach these claimed process steps.

The Examiner combined Lin et al. with Wolf to teach a concept of threshold voltage implanting. The combination of these references still fails to show or suggest the elements of claim 1. Claim 1 also recites that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell, among other elements. Although Wolf could have taught a general concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed.

Accordingly, Claim 1 is patentable over the cited references.

Claim Group 2

The Examiner rejected claims 2 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

Applicants submit that dependent Claim 2 that is dependant from the amended claim 1 is also patentable. The dependent claim 2 is patentable at least for the reasons given above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 2 when combined with independent claim 1. Therefore, Claim 2 is patentable over the cited prior art.

Claim Group 3

The Examiner rejected claims 3 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

The Applicants submit that dependent claim depends from the amended claim 1, and therefore, is also patentable. The dependent claim is patentable at least for the reasons given

above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 3 when combined with independent claim 1. As noted, Claim 3 is also patentable for other reasons.

In particular, Claim 3 further recites that the ions implanted to form the common source region include arsenic ions. The Examiner stated in paragraph 5 on page 3 in the Final Office Action mailed October 20, 2003,

> "Although Lin et al. disclose (col. 6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can bbe readily calculated and implant conditions altered accordingly. *Since the phosphorus diffuses slightly faster than arsenic (page 68), it would be desirable to use arsenic* and therefore obvious to one of ordinary skill in the art at the time of the invention since *both would produce similar results* and thus to combine Sze, Wolf and Lin et al. to obtain ion implant n-type impurities within a flash memory device to form source regions."

Applicants note that the Examiner's statements include arguments that appear inconsistent. In the above statement, the Examiner alleged, "...Since phosphorus diffuses slightly faster than arsenic, it would be desirable to use arsenic ..". But in the "Response to Arguments" the Examiner stated, "...lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling," (paragraph 14, page 10, of the Final Office Action mailed on 10/20/2003). It would then follow that using arsenic instead of phosphorus for source implant in Lin et al. would have resulted in less lateral diffusion and would have decreased the coupling ratio. How could the Examiner state that it would be desirable to use the slower-diffusing arsenic ? The Examiner's arguments appear inconsistent.

As discussed earlier, the coupling ratio in the instant invention is determined by the patterning process which determine the overlap between the floating gate and the source. Because the instant application does not depend on lateral diffusion for increased coupling ratio, arsenic can be advantageously used to make shallow devices.

In addition, Lin et al. clearly taught away from using arsenic in source region implant. For example, Lin at al. stated (Col. 6 lines 42 – 44), "Source implant is accomplished, preferably, by using phosphorous ions." In addition, even though claim 21 of Lin et al. suggested using arsenic for drain region implantation, claim 15 of Lin et al. clearly recited using phosphorus for source region implantation. Accordingly, the combination of Lin et al., Wolf, and Sze not only failed to show or suggest, but actually taught away from, the elements of claim 3 in the instant application. Accordingly, there is no *prima facie* case of obviousness. Therefore, claim 3 is patentable over the cited references.

Claim Group 4

The Examiner rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI ERA: Vol.1 – Process Technology," Lattice Press, Sunset Beach, Ca., (1986), pp. 321 – 322).

Because Claim 4 depends from Claim 1, Applicants believe that claim 4 is allowable for at least the same reasons that claim 1 is allowable. In addition, the Examiner correctly noted that the use of sacrificial oxides is not disclosed. Here, the cited references do not show or suggest the combination of elements included in claim 4 when combined with independent claim 1. Therefore, Claim 4 is patentable over the cited prior art.

Claim Group 5

The Examiner also rejected claims 5 and 9 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 5 and 9 depend from Claim 1, Applicants believe that Claims 5 and 9 are patentable for at least the same reasons that claim 1 is patentable. In addition, Lin et al. and Wolf, taken either separately or in combination, did not disclose or suggestion, at least, " implanting ions into said first and second floating gate regions to adjust said threshold voltage;" and "wherein said ions include Boron ions." Although Wolf could have taught a generally concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed. Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Applicants believe claims 5 and 9 are patentable over the cited references.

Claim Group 6

The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 6 depends from Claim 1, Claim 6 is patentable for at least the same reasons that claim 1 is patentable. In addition, as the Examiner correctly pointed out Lin et al. did not explicitly identify a conductive layer. Wolf also failed to disclose or suggestion, at least, " forming a conductive layer over said second polysilicon layer;.."," Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Claim 6 is patentable over the cited references.

Claim Group 7

The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, further in view of Mizuno ("Hot Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure," IEEE Trans. On Electron Deices, Vol. 38, No. 3, (1991), pp. 584 – 591.)

Because Claim 7 depends from Claim 6, Applicants believe that claim 6 is patentable for at least the same reasons that claim 6 is patentable. In addition, as the Examiner correctly pointed out that Lin et al. did not disclose the composition of the spacer as a nitride. Although Mizunno could have taught a generally concept of nitride spacers, it failed to show or suggest the claim elements of the method for the flash memory device described in Claim 7. Claim 7 recites, *inter alia*, "forming a nitride layer over the first oxide layer, performing an etching process to remove a portion of the nitride layer and leaving nitride spacers adjacent the side walls of each of the floating gates, and forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer,..."

The Examiner alleges that "..it would have been obvious to one of ordinary skill in the art at the time of the invention to use the nitride spacers of Mizuno et al in Lin et al. and to combine Mizuno et al. with Wolf and Lin et al. to obtain appropriate hot carrier suppression." In making this statement, the Examiner fails to realize that a flash memory device utilizes hot carrier injection for programming. Any method for hot carrier suppression would be counterproductive. The Examiner, in fact, produced a motivation to not use the claimed method. Accordingly, Applicant submit that claim 7 is patentable over the cited references.

Claim Group 8

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, and further in view of Wilson ("Handbook of Multilevel Metallization for Integrated Circuits, " Noyes Publ., Westwood, New Jersey, (1993), p. 868).

Because Claim 8 depends from Claim 6, Applicants believe that claim 8 is patentable for at least the same reasons that claim 6 is patentable. In addition, the cited references do not show or suggest the combination of elements included in claim 8 when combined with independent claim 6. Accordingly, Applicant believe that claim 8 is patentable over the cited references.

Claim Group 9

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above.

Because Claim 10 depends from Claim 6, Applicants believe that Claim 10 is patentable for at least the same reasons that claim 6 is patentable. The cited references do not show or suggest the combination of elements included in claim 10 when combined with independent claim 6. Accordingly, Applicants believe that claim 10 is patentable over the cited references.

Claim Group 11

Claim 11 is rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf and further in view of Wolf et al., as applied to Claim 4 above.

Because Claim 11 depends from Claim 4, Claim 11 is patentable for at least the same reasons that claim 4 is patentable. Appicants submit that Claim 11 is also patentable over the cited references for other reasons. Claim 11 recites a method in which implanting ions into the substrate to form the common source region includes implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV. The Examiner combined Wolf, Wolf et al. and Lin et al. to reject claim 11 as unpatentable under 35 U.S.C. 103(a). However, as noted in the previous discussion on claim 3 in Claim Group 2, the combination of Lin et al., Wolf, and Wolf et al. not only failed to show or suggest, but actually taught away from using arsenic in the source region implant as recited in claim 11 in the instant application. Accordingly, Applicants believe claim 11 is patentable over the cited references

Claim Group 12

Claims 12 and 13 are rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf, as applied to Claim 5 above.

Because Claims 12 and 13 depend from Claim 5, Applicants believe that claims 12 and 13 are patentable for at least the same reasons that claim 5 is patentable. In addition, Applicant believe Claims 12 and 13 are patentable for other reasons. For example, Lin et al. did not disclose at least " depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C ..." Accordingly, Claims 12 and 13 are patentable over the cited references.

Claim Group 13

Claims 14 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al.

The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory as recited in the instant application. In the Response to Arguments in the Office Action mailed October 20, 2003, the Examiner also stated that there was no chronology of process steps disclosed in the reference or recited in the claims of the instant application. As discussed earlier, Applicants respectfully submit that the claim 14 has been amended for clarification purposes and demonstrate certain chronology. Claim 14 now recites each floating gate region having a substantial portion overlying the common source region which has a portion that has been implanted with the first ions. Here, implanting ions occurs before forming the floating gates since a substantial portion of the floating gates overlies the implanted portion of

the common source region, the common source region having a portion that has been implanted with the first ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. As discussed earlier, Lin et al. used a completely different process sequence

Therefore, Claim 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Lin falis to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said first ions"

The Examiner also combined Lin et al. with the threshold implants of Wolf, the nitride spacers of Mizuno et al., and the conductive tungsten layers of Wilson et al. to teach a flash memory cell with increased coupling ratio. Applicants assert that the combination of these references fails to show or suggest the claimed combination of elements for fabricating a flash memory device having a high coupling ratio recited in claims 14. As noted earlier, Lin et al. taught a different method of increasing the coupling ratio by using a separate polysilicon layer to provide coupling with the source region, which has nothing to do with Claim 14 of the instant invention.

With regard to threshold implant, lthough Wolf could have taught a generally concept of threshold voltage implanting, the combination of cited prior art still failed to show or suggest the method recited in Claim 14 which includes patterning and etching nitride masking layer to expose at least one first portion and at least one second portion of the first polysilicon layer overlying a portion of the implanted common source region, and implanting ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device.

Similarly, although Mizuno et al. could have taught the general concept of nitride spacers and Wilson et al. could have taught the general concept of using tungsten as a conductive layer, these references in conjunction with Lin et al. still failed to teach the combination of elements in claim 14, which includes, *inter alia,* forming second gate oxide over the first gate oxide layer, over the nitride spacers and over the floating gate oxide layer, forming a second polysilicon layer over the second gate oxide layer, forming a conductive layer over the second polysilicon layer, and removing portions of the conductive layer, second polysilicon layer, second oxide layer, nitride spacers and first gate oxide layer to form a plurality of select gates having a portion overlying a portion of an associated one of the floating gates. As noted earlier, the Examiner actually suggested that Mizuno taught using the nitride spacer to reduce hot carrier effects, whereas in a flash device, it is desirable to enhance hot carrier effects for programming. Thus the cited references teach away from the elements of the instant invention.

With these reasons and as discussed earlier, It is clear that Lin et al. and the other cited references, taken either singly or collectively, failed to show or suggest the combination of claim elements of claim 14. Accordingly, claim 14 is also patentable over the cited references.

Claim Group 14

Claims 16 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14.

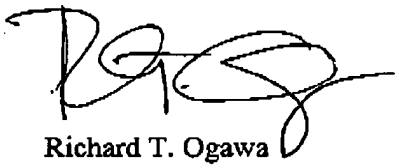
Applicants respectfully disagree. Since claim 16 is dependant from independent claim 14, Claim 16 is patentable for at least the reasons given above. Additionally, the cited references did not show or suggest the claim elements in claim 16, which recites that the first ions include N-type ions and the second ions include P-type ions. Therefore, Applicants submit that claim 16 is patentable over the cited art.

CONCLUSION:

In view of the foregoing arguments distinguishing claims 1–14 and 16 over the art of record, Applicants respectfully submit that claims 1–14 and 16 are in condition for allowance, and respectfully request that and objections to Claims 1 and 14 be removed and the rejection of Claims 1–14 and 16 be reversed.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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Encl.: Appendix of claims involved in appeal

APPENDIX – LISTING OF THE CLAIMS

1. A method of fabricating a flash memory device including an array of split gate cells, comprising:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each pair of said cells;

implanting ions into predefined areas of each said common source region;

forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming drain regions associated with said cells, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming floating gates includes the steps of:

forming a tunneling oxide layer over each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose first and second portions of said first polysilicon layer, said exposed first and second portions substantially define first and second floating gate regions;

implanting ions into said first and second floating gate regions to adjust said threshold voltage;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, said remaining portions of

said first polysilicon layer forming first and second floating gates associated with each said cell, said floating gates having side walls and a portion which overlies a portion of said common source region thereby providing a high coupling ration for the associated cell.

6. A method of fabricating a flash memory device as recited in claim 1 wherein said step of forming said select gates includes the steps of:

forming an insulating layer over the exposed portion of said substrate and the floating gate oxide layer covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form said select gates.

7. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate and said floating gate oxide layer covering said floating gates includes the steps of:

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. A method of fabricating a flash memory device as recited in claim 5, wherein said ions include Boron ions.

10. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming drain regions associated with each cell includes the steps of:

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and

11. A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region includes:

implanting arsenic ions at a dose in the range of 1 x 10^{14} /cm^2 to 5 x 10^{14}/cm^2 and at an energy range of 80 to 150 KeV.

12. A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C in order to form said first layer having a thickness in the range of 500 to 2500 angstroms.

13. A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. A method of fabricating a flash memory device having a high coupling ratio, comprising :

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions, each said floating gate region having a substantial portion thereof overlying said common source region, said common source region having a portion that has been implanted with said first ions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating ate having side walls;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer;

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates;

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least on drain area of said substrate; and

implanting third ions into said drain area of said substrate to form at least one drain region;

whereby the floating gate having a portion which overlies a portion of said common source region thereby providing a high coupling ratio for an associated cell.

15. (Cancelled)

16. A method of fabricating a flash memory device as recited in claim 14, wherein said first ions include N-type ions and said second ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted.

17 – 20. (Withdrawn)

PATENT

Attorney Docket No.: 018757-004600US

I hereby certify that this correspondence is being sent via facsimile to the U.S. Patent Office at (703) 872-9306:

On 4/19/04

TOWNSEND and TOWNSEND and CREW LLP

By: Olivia Elzinga

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chun-Mai Liu et al.

Application No.: 09/827,056

Filed: April 3, 2001

For: METHOD OF FABRICATING HIGH-COUPLING RATIO SPLIT GATE FLASH MEMORY CELL ARRAY

Examiner: Thomas J. Magee

Art Unit: 2811

APPELLANT'S BRIEF UNDER 37 CFR 1.192

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicants appeal the final rejection of claims 1–14 and 16 in the above-captioned patent application. The claims on appeal have been finally rejected pursuant to MPEP 706.07(a). Accordingly, this appeal is proper and is filed in triplicate.

I. REAL PARTY IN INTEREST:

The real party of interest of the above-identified application is Winbond Electronics Corporation, a Taiwan company having its principal place of business at No. 4, Creation Road III, Science-Based Industrial Park, Hsinchu, Taiwan, ROC. The assignment is recorded in the U.S. Patent and Trademark Office on at Reel/Frame 011685/0699.

II. RELATED APPEALS AND INTERFERENCES:

There are no appeals or interferences related to the present appeal.

III. STATUS OF CLAIMS:

Claims 1–14 and 16 are pending and are the subject of this appeal. Claims 1 and 14 are objected to for certain informalities in the Final Office Action dated 10/20/2003. The Examiner stated that ' ... In Claim 1, "said predefined areas having been implanted with said ions," is redundant. Similarly, in Claim 14, the phrase, " ... said common region having a portion that has been implanted with said first ions," is repetitive. Corrections are required.' Applicants respectfully disagree.

All pending claims 1 – 14 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lin et al., (US 6,355,527) in view of what the Examiner indicated was admitted prior art in the same Final Office Action mailed October 20, 2003. Applicants also disagree to the Examiner's rejection.

IV. STATUS OF AMENDMENTS:

There are no amendments filed after the final rejection. In accordance with 37 C.F.R. 1.192 (c) (9), a copy of the claims involved in the appeal is contained in the Appendix attached hereto.

V. SUMMARY OF THE INVENTION:

The present invention relates to a method of fabricating a split gate flash memory device, including cells having an increased coupling ratio thereby reducing the time and voltage required to program each cell. More particularly, the invention also includes threshold voltages adjustment by implanting ions into portions of the substrate defined by the floating gate regions, , to allow for precise threshold voltage control. Details of the claimed method are provided below.

A preferred embodiment of the present invention provides a process of fabricating a flash memory device including an array of split gate cells. The method includes providing a silicon substrate having a top surface and forming a common source region in an area of the top surface for each pair of said cells [Page 5, line 30 to page 6, line 2, and Fig. 2A]. The process requires a certain process sequence for selected steps in the manner claimed. Preferably, the method implants ions into predefined areas of each common source region [Page 6, lines 3 – 15, and Fig. 2B] and then forms floating gates associated with the cells. That is, the formation of the floating gates occurs after implantation of ions into predetermined areas. Each floating gate has a substantial portion thereof overlying one of the predefined areas, which have already been implanted with ions from the previous step of implantation [Page 6, line 16 to page 8, line 3, Figs 2C-2E. The method then forms select gates, each having a first extremity extending over at least a portion of one of the floating gates [Page 8, lines 4-14, Figs. 2F and 2G]. The method also

forms drain regions associated with the cells. Each of the drain regions is positioned proximate a second extremity of one of the select gates [Page 8, lines 15-21, Fig. 2H]. The present process leads to certain benefits associated with the coupling ratio and threshold voltage as will be described in further detail below.

An aspect of the invention relates to a method of forming the floating gates of the flash memory device [Page 6, line 16 to page 8, line 3, Figs 2C-2E]. The method includes forming a tunneling oxide layer over the top surface area of the substrate, depositing a first polysilicon layer over the tunneling oxide layer, and depositing a nitride masking layer over the first polysilicon layer [Page 6, lines 16-24, Fig. 2C]. The process also includes patterning and etching the nitride masking layer to expose first and second portions of the first polysilicon layer, and the exposed first and second portions substantially define first and second floating gate regions [Page 6, lines 24-25, Fig. 2C]. Here the patterning process is used to determine the overlap between the floating gates and the source region [Fig. 2C]. A threshold implantation step occurs after the patterning process.

Specifically, the method then implants ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of the common source region, in order to adjust the threshold voltage of the flash memory device [Page 6, lines 26-31]. This implanting step allows precise control of threshold implant under the floating gate. The method continues with forming a floating gate oxide layer over the first and second exposed portions of the first polysilicon layer [Page 7, lines 5-11, Fig. 2D]. After removing the nitride masking layer, the method then etches the first polysilicon layer and the tunneling oxide layer using the floating gate oxide layer as a mask. This method leaves remaining portions of the first polysilicon layer and the tunneling oxide layer disposed beneath said floating gate oxide layer, and exposes a portion of the substrate. The remaining portions of the first polysilicon layer form first and second floating gates associated with each cell. These floating gates have side walls and a portion which overlies a portion of the common source region, thereby providing a high coupling ration for the associated cell [Page 7, lines 13-18, Figs. 2D and 2E]. As described earlier, determines the extent of the overlap and, therefore, the coupling ratio [Fig. 2C-2E].

Using the specific process of the present invention, certain benefits are achieved over conventional techniques. The present process is easy to use and avoids certain processing difficulties of the prior art. Additionally, the step of implanting ions into each of the predefined first and second floating gate regions adjusts the channel threshold voltage to provide precise threshold voltages [Page 3, lines 27 – 31]. The step of forming the floating gates after implanting the source region allows the floating gate patterning step to determine the desired overlap between the floating gate and the source region, and, as a result, provides a high coupling ratio for the associated flash cells. In contrast, in conventional devices the coupling between source and floating is limited by the side diffusion of the ions implanted after the floating gate formation [Page 2, line 24 to page 3, line 26]. The high coupling ratio allows for improved programming of the present flash memory device and reduces the time and voltage

required to program each cell. These and other benefits will be described throughout the present appeal and more particularly below.

VI. ISSUES

The following issues are presented:

1. Whether the Examiner properly objected to claims 1 and 14.
2. Whether claims 1 –1 4 and 16 were properly rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of what the Examiner considers admitted prior art.

VII. GROUPING OF THE CLAIMS:

In the present case, the rejected claims do not all stand or fall together. Applicants submit that certain claims present distinct issues concerning patentability. For purposes of preserving these distinct issues, Applicants group the claims as follows.

Group 1: Claim 1, which stands or falls by itself.

Group 2: Claim 2, which stands or falls by itself.

Group 3: Claim 3, which stands or falls by itself.

Group 4: Claim 4, which stands or falls by itself.

Group 5: Claims 5 and 9, which stand or fall together.

Claim 6: Claim 6, which stands or falls by itself.

Group 7: Claim 7, which stands or falls by itself.

Group 8: Claim 8, which stands or falls by itself.

Group 9: Claim 10, which stands or falls by itself.

Group 10. Claim 11, which stands or falls by itself.

Group 11: Claims 12 and 13, which stand or fall together.

Group 12: Claim 14, which stands or falls by itself.

Group 13: Claim 16, which stands or falls by itself.

VIII. ARGUMENTS:

Because all the claims do not stand or fall together, Applicants present arguments for each claim group later in this brief. Before specifically discussing the Examiner's rejection as applied to each of the claim groups, Applicants first address the Examiner's basis for maintaining the rejection which was applied to all pending claims.

Improper Basis For Rejections

The Examiner has not appreciated that the invention of claims 1 and 14 require a certain chronology of steps. In the Final Office Action mailed October 20, 2003, the Examiner summarized the grounds for maintaining the rejection of claims 1 – 14 and 16 under 35 U.S.C. 103(a) in paragraph 14 on pages 9 and 10, as follows:

> "With regard to Independent Claims 1 and 14, Examiner must again reiterate that he can only interpret language posed in limitations of claims and currently, Lin et al. discloses those tenets recited in the claims of the instant application of Applicant. *There is no chronology of process steps disclosed in the reference or recited in the claims of the instant application.* Therefore, arguments appear moot." [Emphasis Added.]

Applicants respectfully submit that the claims 1 and 14 are patentable over the cited references. As noted earlier and further emphasized herein, claims 1 and 14 recite a certain sequence of steps requiring a chronology, which the Examiner has not appreciated. Using claim 1 as an example, it recites, *inter alia,*

> "*forming a common source region* in an area of said top surface for each pair of said cells;
>
> *implanting ions into predefined areas of each said common source region;*
>
> *forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions; ...*"

Since the floating gate is formed to overlie the predefined area, and the predefined area "has been implanted with said ions", it is clear that ion implantation into the common source region precedes the floating gate formation, such that a substantial portion of the floating gates overlies the implanted common source region in the substrate that has been implanted with the ions. Here, forming the floating gates occurs after the predefined area has already been implanted with ions, so that a substantial portion of the floating gate is formed to overlie the implanted common source region.

Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. In contrast, Lin et al. used a completely different process sequence. Column 6 lines 26 – 28 of Lin et al. stated, "source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." Further, Claim 1of Lin et al. (US 6,355,527) recites, inter alia,

> " ... etching said first polysilicon layer to form said floating gate using said regions of poly-oxide as a hard mask; **then**
>
> forming a second photoresist layer over said substrate and patterning to define source region; **then**
>
> performing ion implantation through openings in said second photoresist layer to form source region, ...; **then ...**"

The Examiner is mistaken in stating that: "no chronology of process steps disclosed in the reference or recited in the claims of the instant application." (Paragraph 14, Response to Arguments in the 10/20/2003 Office Action) As noted above, Lin et al. discloses the sequences of etching the first polysilicon layer, then forming a second photoresist, and then performing ion implantation, which are not the inventions of claims 1 and 14. Accordingly, claims 1 and 14 are patentable over Lin et al.

The Examiner also misunderstands how the "coupling ratio" is increased by Lin et al. and the invention of claims 1 and 14. The Examiner stated,

> " The lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling."

The Examiner further stated,

> "Applicant has apparently misread in reference, since the coupling ratio is due to the Distance source extends beneath gate, as claimed in the reference and also recited in the instant application."

Applicants note that, since the device in Lin et al. is formed with source implant after the floating gate formation, the coupling between source and floating gate is provided by lateral diffusion of source beneath gate. This side diffusion is limited, because the maximum allowable diffusion depth of the common source region is limited (See, specification of the instant invention, page 4 lines 23 – 30). Under such limitation, Lin et al. sought to obtain higher coupling ratio by coupling the floating gate with an extra polysilicon line. Lin et al. stated, "The main feature of the invention, ... to form a poly line (165) continuous over the source region (125')..." (Col. 6, lines 51 – 58) and " ... the poly line provides an additional vertical wall area along the edges of the floating gates (140). The additional area shares the voltage levels imposed between source (125) and the floating gate (140),...by virtue of the increased sidewall coupling area between the source and the floating gate , the coupling ratio is also increased..." (Col. 6, lines 64 – Col. 7 ,

line3). In contrast, the invention of claims 1 and 14 recites a different method for achieving higher coupling ratio.

The high coupling ratio flash cell device of the present invention overcomes the side-diffusion coupling limitation by forming the implanted common source region first, and then forming the floating gates (See, specification of the instant invention, page 4 lines 23 – 30). In this case, the extent of overlap of the floating gate over the implanted common source region is determined by the patterning process (page 6, line 16 to page 7, line 18, and figs 2C – 2E), instead of side diffusion. This pont is further explained in the Applicants' specification, page 8, line 27 – page 9 line 2, "The device 200 provides cells having an increased source side coupling ratio relative to the prior art. The increased source side coupling ratio is due to the distance 202 the source region extends beneath the floating gate 124A, 124B being increase over the distance 46 the prior art source region 42 (Fig. 1) extends beneath floating gate 22, 24 (Fig. 1). This increases in the distance the source region 116 extends beneath the floating gate 124A. 124B is provided by the method of the present invention."

Accordingly, the invention as recited in Claim 1 and 14 of the instant application provides a method to increase the extent of the overlap between source and floating gate without increasing the lateral diffusion and the diffusion depth of the source, thus providing an increased coupling ratio. Lin et al. does not show or suggest these claimed features. Therefore, claims 1 and 14 are patentable over Lin et al.

Claim Objections

The Examiner objected to claims 1 and 14 in the Final Office Action mailed October 20, 2003,

"In Claim 1, the recitation, 'said predefined areas having been implanted with said ion,' is redundant. Similarly, in Claim 14, the phrase, '.... said common source region having a portion that has been implanted with said first ions,' is repetitive. Corrections are required."

Applicants note that the recitations were introduced in Applicants' 08/18/2003 amendment for the purpose of clarifying the chronology of the process sequence, in response to the 6/18/2003 Office Action But as discussed earlier, the Examiner still fails to appreciate the chronology and regarded these phrases redundant and repetitive. Applicants submit that with the amendment of the recitation, "said predefined areas having been implanted with said ion," in claim 1, it is now clear that the floating gate is formed after the common source region has been formed and has been implanted with the ions, because the floating gate has a substantial portion overlying the area which has been implanted with the ions. Similarly, in claim 14, the recitation, "'.... said common source region having a portion that has been implanted with said first ions," further clarifies that the floating gate is formed after the common source region has been formed and has been implanted with the ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed.

Therefore, claims 1 and 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Applicants request that the Examiner's objections to Claims 1 and 14 be removed.

Rejection of claims under § 103(a)

The Examiner rejected Claims 1 – 14 and 6 under 35 U.S.C. 103(a) as unpatentable over Lin et al. (US 6,355,527) in view of wht the Examiner considers admitted prior art. Applicants respectfully traverse the rejection of these claims.

To establish a *prima facie* case of obviousness under §103(a), each of three requirements must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine references or modify a reference. (MPEP § 2143.01.) Second, a reasonable expectation of success must exist that the proposed modification will work for the intended purpose. (MPEP § 2143.02.) Moreover, both of these requirements must "be found in the prior art, not in applicant's disclosure." (MPEP § 2142.) Third, the reference or references, taken alone or in combination, must disclose or suggest every element recited in the claims. (MPEP §2143.03.)

Because all the claims do not stand or fall together, Applicants will present argument for each claim groups.

Claim Group 1

The Examiner has maintained his rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI ERA: Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322). Here, the Examiner suggested that Lin et al. disclosed a method for forming split-gate flash memories with improved, increased coupling ratio and that Wolf, pp. 321 – 322, showed adjustment of channel threshold voltage using ion implantation. The Applicants disagree with the Examiner's argument.

In rejecting Claim 1, the Examiner stated in the 10/20/2003 Office Action,

> "Regarding Claim 1, Lin et al. clearly disclose a method for forming split-gate flash memories with improved, increased coupling ratio. A common source region is formed (125) (Figure 2G) in a silicon substrate. Source implantation is done using n-type implants (Col. 6 lines 42 – 45) and drains (120) implanted at opposite sides of the source (and within the vicinity (second extremity) of gate regions) (Figure 2G) using n-type implants (Col 7, lines 14 – 18). Floating gates (140) (Figure 2D) are formed, overlying areas of the common source region (Figure 2D) and extremities extending over the (first) part of the structure."

It appears that the Examiner ignored the chronology in Lin's disclosure, both in the specification and claims, which forms the floating gate before the source region implant, , as discussed earlier, Also as discussed earlier, Claim 1 of the instant invention clearly demonstrate a chronology. Claim 1 now recites floating gate formation after ion implantation into the common source region , such that a substantial portion of the floating gates overlies the implanted common source region in the substrate. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. Lin fails to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions." Wolf also failed to teach these claimed process steps.

The Examiner combined Lin et al. with Wolf to teach a concept of threshold voltage implanting. The combination of these references still fails to show or suggest the elements of claim 1. Claim 1 also recites that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell, among other elements. Although Wolf could have taught a general concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed.

Accordingly, Claim 1 is patentable over the cited references.

Claim Group 2

The Examiner rejected claims 2 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

Applicants submit that dependent Claim 2 that is dependant from the amended claim 1 is also patentable. The dependent claim 2 is patentable at least for the reasons given above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 2 when combined with independent claim 1. Therefore, Claim 2 is patentable over the cited prior art.

Claim Group 3

The Examiner rejected claims 3 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

The Applicants submit that dependent claim depends from the amended claim 1, and therefore, is also patentable. The dependent claim is patentable at least for the reasons given

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above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 3 when combined with independent claim 1. As noted, Claim 3 is also patentable for other reasons.

In particular, Claim 3 further recites that the ions implanted to form the common source region include arsenic ions. The Examiner stated in paragraph 5 on page 3 in the Final Office Action mailed October 20, 2003,

"Although Lin et al. disclose (col. 6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can bbe readily calculated and implant conditions altered accordingly. *Since the phosphorus diffuses slightly faster than arsenic (page 68), it would be desirable to use arsenic* and therefore obvious to one of ordinary skill in the art at the time of the invention since *both would produce similar results* and thus to combine Sze, Wolf and Lin et al. to obtain ion implant n-type impurities within a flash memory device to form source regions."

Applicants note that the Examiner's statements include arguments that appear inconsistent. In the above statement, the Examiner alleged, "...Since phosphorus diffuses slightly faster than arsenic, it would be desirable to use arsenic ..". But in the "Response to Arguments" the Examiner stated, "...lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling," (paragraph 14, page 10, of the Final Office Action mailed on 10/20/2003). It would then follow that using arsenic instead of phosphorus for source implant in Lin et al. would have resulted in less lateral diffusion and would have decreased the coupling ratio. How could the Examiner state that it would be desirable to use the slower-diffusing arsenic ? The Examiner's arguments appear inconsistent.

As discussed earlier, the coupling ratio in the instant invention is determined by the patterning process which determine the overlap between the floating gate and the source. Because the instant application does not depend on lateral diffusion for increased coupling ratio, arsenic can be advantageously used to make shallow devices.

In addition, Lin et al. clearly taught away from using arsenic in source region implant. For example, Lin at al. stated (Col. 6 lines 42 – 44), "Source implant is accomplished, preferably, by using phosphorous ions." In addition, even though claim 21 of Lin et al. suggested using arsenic for drain region implantation, claim 15 of Lin et al. clearly recited using phosphorus for source region implantation. Accordingly, the combination of Lin et al., Wolf, and Sze not only failed to show or suggest, but actually taught away from, the elements of claim 3 in the instant application. Accordingly, there is no *prima facie* case of obviousness. Therefore, claim 3 is patentable over the cited references.

Claim Group 4

The Examiner rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI ERA: Vol.1 – Process Technology," Lattice Press, Sunset Beach, Ca., (1986), pp. 321 – 322).

Because Claim 4 depends from Claim 1, Applicants believe that claim 4 is allowable for at least the same reasons that claim 1 is allowable. In addition, the Examiner correctly noted that the use of sacrificial oxides is not disclosed. Here, the cited references do not show or suggest the combination of elements included in claim 4 when combined with independent claim 1. Therefore, Claim 4 is patentable over the cited prior art.

Claim Group 5

The Examiner also rejected claims 5 and 9 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 5 and 9 depend from Claim 1, Applicants believe that Claims 5 and 9 are patentable for at least the same reasons that claim 1 is patentable. In addition, Lin et al. and Wolf, taken either separately or in combination, did not disclose or suggestion, at least, " implanting ions into said first and second floating gate regions to adjust said threshold voltage;" and "wherein said ions include Boron ions." Although Wolf could have taught a generally concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed. Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Applicants believe claims 5 and 9 are patentable over the cited references.

Claim Group 6

The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 6 depends from Claim 1, Claim 6 is patentable for at least the same reasons that claim 1 is patentable. In addition, as the Examiner correctly pointed out Lin et al. did not explicitly identify a conductive layer. Wolf also failed to disclose or suggestion, at least, " forming a conductive layer over said second polysilicon layer;.." Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Claim 6 is patentable over the cited references.

Claim Group 7

The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, further in view of Mizuno ("Hot Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure," IEEE Trans. On Electron Deices, Vol. 38, No. 3, (1991), pp. 584 – 591.)

Because Claim 7 depends from Claim 6, Applicants believe that claim 6 is patentable for at least the same reasons that claim 6 is patentable. In addition, as the Examiner correctly pointed out that Lin et al. did not disclose the composition of the spacer as a nitride. Although Mizunno could have taught a generally concept of nitride spacers, it failed to show or suggest the claim elements of the method for the flash memory device described in Claim 7. Claim 7 recites, *inter alia*, "forming a nitride layer over the first oxide layer, performing an etching process to remove a portion of the nitride layer and leaving nitride spacers adjacent the side walls of each of the floating gates, and forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer,..."

The Examiner alleges that "..it would have been obvious to one of ordinary skill in the art at the time of the invention to use the nitride spacers of Mizuno et al in Lin et al. and to combine Mizuno et al. with Wolf and Lin et al. to obtain appropriate hot carrier suppression." In making this statement, the Examiner fails to realize that a flash memory device utilizes hot carrier injection for programming. Any method for hot carrier suppression would be counterproductive. The Examiner, in fact, produced a motivation to not use the claimed method. Accordingly, Applicant submit that claim 7 is patentable over the cited references.

Claim Group 8

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, and further in view of Wilson ("Handbook of Multilevel Metallization for Integrated Circuits, " Noyes Publ., Westwood, New Jersey, (1993), p. 868).

Because Claim 8 depends from Claim 6, Applicants believe that claim 8 is patentable for at least the same reasons that claim 6 is patentable. In addition, the cited references do not show or suggest the combination of elements included in claim 8 when combined with independent claim 6. Accordingly, Applicant believe that claim 8 is patentable over the cited references.

Claim Group 9

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above.

Because Claim 10 depends from Claim 6, Applicants believe that Claim 10 is patentable for at least the same reasons that claim 6 is patentable. The cited references do not show or suggest the combination of elements included in claim 10 when combined with independent claim 6. Accordingly, Applicants believe that claim 10 is patentable over the cited references.

Claim Group 11

Claim 11 is rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf and further in view of Wolf et al., as applied to Claim 4 above.

Because Claim 11 depends from Claim 4, Claim 11 is patentable for at least the same reasons that claim 4 is patentable. Appicants submit that Claim 11 is also patentable over the cited references for other reasons. Claim 11 recites a method in which implanting ions into the substrate to form the common source region includes implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV. The Examiner combined Wolf, Wolf et al. and Lin et al. to reject claim 11 as unpatentable under 35 U.S.C. 103(a). However, as noted in the previous discussion on claim 3 in Claim Group 2, the combination of Lin et al., Wolf, and Wolf et al. not only failed to show or suggest, but actually taught away from using arsenic in the source region implant as recited in claim 11 in the instant application. Accordingly, Applicants believe claim 11 is patentable over the cited references

Claim Group 12

Claims 12 and 13 are rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf, as applied to Claim 5 above.

Because Claims 12 and 13 depend from Claim 5, Applicants believe that claims 12 and 13 are patentable for at least the same reasons that claim 5 is patentable. In addition, Applicant believe Claims 12 and 13 are patentable for other reasons. For example, Lin et al. did not disclose at least " depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C ..." Accordingly, Claims 12 and 13 are patentable over the cited references.

Claim Group 13

Claims 14 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al.

The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory as recited in the instant application. In the Response to Arguments in the Office Action mailed October 20, 2003, the Examiner also stated that there was no chronology of process steps disclosed in the reference or recited in the claims of the instant application. As discussed earlier, Applicants respectfully submit that the claim 14 has been amended for clarification purposes and demonstrate certain chronology. Claim 14 now recites each floating gate region having a substantial portion overlying the common source region which has a portion that has been implanted with the first ions. Here, implanting ions occurs before forming the floating gates since a substantial portion of the floating gates overlies the implanted portion of

the common source region, the common source region having a portion that has been implanted with the first ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. As discussed earlier, Lin et al. used a completely different process sequence

Therefore, Claim 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Lin falis to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said first ions"

The Examiner also combined Lin et al. with the threshold implants of Wolf, the nitride spacers of Mizuno et al., and the conductive tungsten layers of Wilson et al. to teach a flash memory cell with increased coupling ratio. Applicants assert that the combination of these references fails to show or suggest the claimed combination of elements for fabricating a flash memory device having a high coupling ratio recited in claims 14. As noted earlier, Lin et al. taught a different method of increasing the coupling ratio by using a separate polysilicon layer to provide coupling with the source region, which has nothing to do with Claim 14 of the instant invention.

With regard to threshold implant, lthough Wolf could have taught a generally concept of threshold voltage implanting, the combination of cited prior art still failed to show or suggest the method recited in Claim 14 which includes patterning and etching nitride masking layer to expose at least one first portion and at least one second portion of the first polysilicon layer overlying a portion of the implanted common source region, and implanting ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device.

Similarly, although Mizuno et al. could have taught the general concept of nitride spacers and Wilson et al. could have taught the general concept of using tungsten as a conductive layer, these references in conjunction with Lin et al. still failed to teach the combination of elements in claim 14, which includes, *inter alia,* forming second gate oxide over the first gate oxide layer, over the nitride spacers and over the floating gate oxide layer, forming a second polysilicon layer over the second gate oxide layer, forming a conductive layer over the second polysilicon layer, and removing portions of the conductive layer, second polysilicon layer, second oxide layer, nitride spacers and first gate oxide layer to form a plurality of select gates having a portion overlying a portion of an associated one of the floating gates. As noted earlier, the Examiner actually suggested that Mizuno taught using the nitride spacer to reduce hot carrier effects, whereas in a flash device, it is desirable to enhance hot carrier effects for programming. Thus the cited references teach away from the elements of the instant invention.

With these reasons and as discussed earlier, It is clear that Lin et al. and the other cited refcrences, taken either singly or collcctively, failed to show or suggest the combination of claim elements of claim 14. Accordingly, claim 14 is also patentable over the cited references.

Claim Group 14

Claims 16 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14.

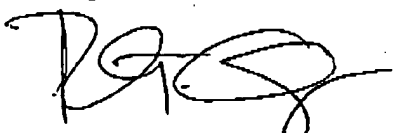
Applicants respectfully disagree. Since claim 16 is dependant from independent claim 14, Claim 16 is patentable for at least the reasons given above. Additionally, the cited references did not show or suggest the claim elements in claim 16, which recites that the first ions include N-type ions and the second ions include P-type ions. Therefore, Applicants submit that claim 16 is patentable over the cited art.

CONCLUSION:

In view of the foregoing arguments distinguishing claims 1–14 and 16 over the art of record, Applicants respectfully submit that claims 1–14 and 16 are in condition for allowance, and respectfully request that and objections to Claims 1 and 14 be removed and the rejection of Claims 1–14 and 16 be reversed.

If the Examincr believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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Encl.: Appendix of claims involved in appeal

APPENDIX – LISTING OF THE CLAIMS

1. A method of fabricating a flash memory device including an array of split gate cells, comprising:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each pair of said cells;

implanting ions into predefined areas of each said common source region;

forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming drain regions associated with said cells, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming floating gates includes the steps of:

forming a tunneling oxide layer over each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose first and second portions of said first polysilicon layer, said exposed first and second portions substantially define first and second floating gate regions;

implanting ions into said first and second floating gate regions to adjust said threshold voltage;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, said remaining portions of

said first polysilicon layer forming first and second floating gates associated with each said cell, said floating gates having side walls and a portion which overlies a portion of said common source region thereby providing a high coupling ration for the associated cell.

6. A method of fabricating a flash memory device as recited in claim 1 wherein said step of forming said select gates includes the steps of:

forming an insulating layer over the exposed portion of said substrate and the floating gate oxide layer covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form said select gates.

7. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate and said floating gate oxide layer covering said floating gates includes the steps of:

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. A method of fabricating a flash memory device as recited in claim 5, wherein said ions include Boron ions.

10. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming drain regions associated with each cell includes the steps of:

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and

11. A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region includes:

implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV.

12. A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C in order to form said first layer having a thickness in the range of 500 to 2500 angstroms.

13. A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. A method of fabricating a flash memory device having a high coupling ratio, comprising :

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions, each said floating gate region having a substantial portion thereof overlying said common source region, said common source region having a portion that has been implanted with said first ions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating ate having side walls;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer;

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates;

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least on drain area of said substrate; and

implanting third ions into said drain area of said substrate to form at least one drain region;

whereby the floating gate having a portion which overlies a portion of said common source region thereby providing a high coupling ratio for an associated cell.

15. (Cancelled)

16. A method of fabricating a flash memory device as recited in claim 14, wherein said first ions include N-type ions and said second ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted.

17 – 20. (Withdrawn)

PATENT

I hereby certify that this correspondence is being sent via facsimile to the U.S. Patent Office at (703) 872-9306:

On 4/19/04

TOWNSEND and TOWNSEND and CREW LLP

By: Diane Elzinga

Attorney Docket No.: 018757-004600US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chun-Mai Liu et al.

Application No.: 09/827,056

Filed: April 3, 2001

For: METHOD OF FABRICATING HIGH-COUPLING RATIO SPLIT GATE FLASH MEMORY CELL ARRAY

Examiner: Thomas J. Magee

Art Unit: 2811

APPELLANT'S BRIEF UNDER 37 CFR 1.192

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicants appeal the final rejection of claims 1–14 and 16 in the above-captioned patent application. The claims on appeal have been finally rejected pursuant to MPEP 706.07(a). Accordingly, this appeal is proper and is filed in triplicate.

I. REAL PARTY IN INTEREST:

The real party of interest of the above-identified application is Winbond Electronics Corporation, a Taiwan company having its principal place of business at No. 4, Creation Road III, Science-Based Industrial Park, Hsinchu, Taiwan, ROC. The assignment is recorded in the U.S. Patent and Trademark Office on at Reel/Frame 011685/0699.

II. RELATED APPEALS AND INTERFERENCES:

There are no appeals or interferences related to the present appeal.

III. STATUS OF CLAIMS:

Claims 1–14 and 16 are pending and are the subject of this appeal. Claims 1 and 14 are objected to for certain informalities in the Final Office Action dated 10/20/2003. The Examiner stated that ' ... In Claim 1, "said predefined areas having been implanted with said ions," is redundant. Similarly, in Claim 14, the phrase, " ... said common region having a portion that has been implanted with said first ions," is repetitive. Corrections are required.' Applicants respectfully disagree.

All pending claims 1 – 14 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lin et al., (US 6,355,527) in view of what the Examiner indicated was admitted prior art in the same Final Office Action mailed October 20, 2003. Applicants also disagree to the Examiner's rejection.

IV. STATUS OF AMENDMENTS:

There are no amendments filed after the final rejection. In accordance with 37 C.F.R. 1.192 (c) (9), a copy of the claims involved in the appeal is contained in the Appendix attached hereto.

V. SUMMARY OF THE INVENTION:

The present invention relates to a method of fabricating a split gate flash memory device, including cells having an increased coupling ratio thereby reducing the time and voltage required to program each cell. More particularly, the invention also includes threshold voltages adjustment by implanting ions into portions of the substrate defined by the floating gate regions, , to allow for precise threshold voltage control. Details of the claimed method are provided below.

A preferred embodiment of the present invention provides a process of fabricating a flash memory device including an array of split gate cells. The method includes providing a silicon substrate having a top surface and forming a common source region in an area of the top surface for each pair of said cells [Page 5, line 30 to page 6, line 2, and Fig. 2A]. The process requires a certain process sequence for selected steps in the manner claimed. Preferably, the method implants ions into predefined areas of each common source region [Page 6, lines 3 – 15, and Fig. 2B] and then forms floating gates associated with the cells. That is, the formation of the floating gates occurs after implantation of ions into predetermined areas. Each floating gate has a substantial portion thereof overlying one of the predefined areas, which have already been implanted with ions from the previous step of implantation [Page 6, line 16 to page 8, line 3, Figs 2C-2E. The method then forms select gates, each having a first extremity extending over at least a portion of one of the floating gates [Page 8, lines 4-14, Figs. 2F and 2G]. The method also

forms drain regions associated with the cells. Each of the drain regions is positioned proximate a second extremity of one of the select gates [Page 8, lines 15-21, Fig. 2H]. The present process leads to certain benefits associated with the coupling ratio and threshold voltage as will be described in further detail below.

An aspect of the invention relates to a method of forming the floating gates of the flash memory device [Page 6, line 16 to page 8, line 3, Figs 2C-2E]. The method includes forming a tunneling oxide layer over the top surface area of the substrate, depositing a first polysilicon layer over the tunneling oxide layer, and depositing a nitride masking layer over the first polysilicon layer [Page 6, lines 16-24, Fig. 2C]. The process also includes patterning and etching the nitride masking layer to expose first and second portions of the first polysilicon layer, and the exposed first and second portions substantially define first and second floating gate regions [Page 6, lines 24-25, Fig. 2C]. Here the patterning process is used to determine the overlap between the floating gates and the source region [Fig. 2C]. A threshold implantation step occurs after the patterning process.

Specifically, the method then implants ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of the common source region, in order to adjust the threshold voltage of the flash memory device [Page 6, lines 26-31]. This implanting step allows precise control of threshold implant under the floating gate. The method continues with forming a floating gate oxide layer over the first and second exposed portions of the first polysilicon layer [Page 7, lines 5-11, Fig. 2D]. After removing the nitride masking layer, the method then etches the first polysilicon layer and the tunneling oxide layer using the floating gate oxide layer as a mask. This method leaves remaining portions of the first polysilicon layer and the tunneling oxide layer disposed beneath said floating gate oxide layer, and exposes a portion of the substrate. The remaining portions of the first polysilicon layer form first and second floating gates associated with each cell. These floating gates have side walls and a portion which overlies a portion of the common source region, thereby providing a high coupling ration for the associated cell [Page 7, lines 13-18, Figs. 2D and 2E]. As described earlier, determines the extent of the overlap and, therefore, the coupling ratio [Fig. 2C-2E].

Using the specific process of the present invention, certain benefits are achieved over conventional techniques. The present process is easy to use and avoids certain processing difficulties of the prior art. Additionally, the step of implanting ions into each of the predefined first and second floating gate regions adjusts the channel threshold voltage to provide precise threshold voltages [Page 3, lines 27 – 31]. The step of forming the floating gates after implanting the source region allows the floating gate patterning step to determine the desired overlap between the floating gate and the source region, and, as a result, provides a high coupling ratio for the associated flash cells. In contrast, in conventional devices the coupling between source and floating is limited by the side diffusion of the ions implanted after the floating gate formation [Page 2, line 24 to page 3, line 26]. The high coupling ratio allows for improved programming of the present flash memory device and reduces the time and voltage

required to program each cell. These and other benefits will be described throughout the present appeal and more particularly below.

VI. ISSUES

The following issues are presented:

1. Whether the Examiner properly objected to claims 1 and 14.
2. Whether claims 1 –1 4 and 16 were properly rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of what the Examiner considers admitted prior art.

VII. GROUPING OF THE CLAIMS:

In the present case, the rejected claims do not all stand or fall together. Applicants submit that certain claims present distinct issues concerning patentability. For purposes of preserving these distinct issues, Applicants group the claims as follows.

Group 1: Claim 1, which stands or falls by itself.

Group 2: Claim 2, which stands or falls by itself.

Group 3: Claim 3, which stands or falls by itself.

Group 4: Claim 4, which stands or falls by itself.

Group 5: Claims 5 and 9, which stand or fall together.

Claim 6: Claim 6, which stands or falls by itself.

Group 7: Claim 7, which stands or falls by itself.

Group 8: Claim 8, which stands or falls by itself.

Group 9: Claim 10, which stands or falls by itself.

Group 10. Claim 11, which stands or falls by itself.

Group 11: Claims 12 and 13, which stand or fall together.

Group 12: Claim 14, which stands or falls by itself.

Group 13: Claim 16, which stands or falls by itself.

VIII. ARGUMENTS:

Because all the claims do not stand or fall together, Applicants present arguments for each claim group later in this brief. Before specifically discussing the Examiner's rejection as applied to each of the claim groups, Applicants first address the Examiner's basis for maintaining the rejection which was applied to all pending claims.

Improper Basis For Rejections

The Examiner has not appreciated that the invention of claims 1 and 14 require a certain chronology of steps. In the Final Office Action mailed October 20, 2003, the Examiner summarized the grounds for maintaining the rejection of claims 1 – 14 and 16 under 35 U.S.C. 103(a) in paragraph 14 on pages 9 and 10, as follows:

> "With regard to Independent Claims 1 and 14, Examiner must again reiterate that he can only interpret language posed in limitations of claims and currently, Lin et al. discloses those tenets recited in the claims of the instant application of Applicant. *There is no chronology of process steps disclosed in the reference or recited in the claims of the instant application.* Therefore, arguments appear moot." [Emphasis Added.]

Applicants respectfully submit that the claims 1 and 14 are patentable over the cited references. As noted earlier and further emphasized herein, claims 1 and 14 recite a certain sequence of steps requiring a chronology, which the Examiner has not appreciated. Using claim 1 as an example, it recites, *inter alia,*

> "*forming a common source region* in an area of said top surface for each pair of said cells;
>
> *implanting ions into predefined areas of each said common source region;*
>
> *forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions; ...*"

Since the floating gate is formed to overlie the predefined area, and the predefined area "has been implanted with said ions", it is clear that ion implantation into the common source region precedes the floating gate formation, such that a substantial portion of the floating gates overlies the implanted common source region in the substrate that has been implanted with the ions. Here, forming the floating gates occurs after the predefined area has already been implanted with ions, so that a substantial portion of the floating gate is formed to overlie the implanted common source region.

Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. In contrast, Lin et al. used a completely different process sequence. Column 6 lines 26 – 28 of Lin et al. stated, "source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." Further, Claim 1of Lin et al. (US 6,355,527) recites, inter alia,

> " ... etching said first polysilicon layer to form said floating gate using said regions of poly-oxide as a hard mask; **then**
>
> forming a second photoresist layer over said substrate and patterning to define source region; **then**
>
> performing ion implantation through openings in said second photoresist layer to form source region, ...; **then ...**"

The Examiner is mistaken in stating that: "no chronology of process steps disclosed in the reference or recited in the claims of the instant application." (Paragraph 14, Response to Arguments in the 10/20/2003 Office Action) As noted above, Lin et al. discloses the sequences of etching the first polysilicon layer, then forming a second photoresist, and then performing ion implantation, which are not the inventions of claims 1 and 14. Accordingly, claims 1 and 14 are patentable over Lin et al.

The Examiner also misunderstands how the "coupling ratio" is increased by Lin et al. and the invention of claims 1 and 14. The Examiner stated,

> " The lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling."

The Examiner further stated,

> "Applicant has apparently misread in reference, since the coupling ratio is due to the Distance source extends beneath gate, as claimed in the reference and also recited in the instant application."

Applicants note that, since the device in Lin et al. is formed with source implant after the floating gate formation, the coupling between source and floating gate is provided by lateral diffusion of source beneath gate. This side diffusion is limited, because the maximum allowable diffusion depth of the common source region is limited (See, specification of the instant invention, page 4 lines 23 – 30). Under such limitation, Lin et al. sought to obtain higher coupling ratio by coupling the floating gate with an extra polysilicon line. Lin et al. stated, "The main feature of the invention, ... to form a poly line (165) continuous over the source region (125')..." (Col. 6, lines 51 – 58) and " ... the poly line provides an additional vertical wall area along the edges of the floating gates (140). The additional area shares the voltage levels imposed between source (125) and the floating gate (140),...by virtue of the increased sidewall coupling area between the source and the floating gate , the coupling ratio is also increased..." (Col. 6, lines 64 – Col. 7 ,

line3). In contrast, the invention of claims 1 and 14 recites a different method for achieving higher coupling ratio.

The high coupling ratio flash cell device of the present invention overcomes the side-diffusion coupling limitation by forming the implanted common source region first, and then forming the floating gates (See, specification of the instant invention, page 4 lines 23 – 30). In this case, the extent of overlap of the floating gate over the implanted common source region is determined by the patterning process (page 6, line 16 to page 7, line 18, and figs 2C – 2E), instead of side diffusion. This pont is further explained in the Applicants' specification, page 8, line 27 – page 9 line 2, "The device 200 provides cells having an increased source side coupling ratio relative to the prior art. The increased source side coupling ratio is due to the distance 202 the source region extends beneath the floating gate 124A, 124B being increase over the distance 46 the prior art source region 42 (Fig. 1) extends beneath floating gate 22, 24 (Fig. 1). This increases in the distance the source region 116 extends beneath the floating gate 124A. 124B is provided by the method of the present invention."

Accordingly, the invention as recited in Claim 1 and 14 of the instant application provides a method to increase the extent of the overlap between source and floating gate without increasing the lateral diffusion and the diffusion depth of the source, thus providing an increased coupling ratio. Lin et al. does not show or suggest these claimed features. Therefore, claims 1 and 14 are patentable over Lin et al.

Claim Objections

The Examiner objected to claims 1 and 14 in the Final Office Action mailed October 20, 2003,

"In Claim 1, the recitation, 'said predefined areas having been implanted with said ion,' is redundant. Similarly, in Claim 14, the phrase, '.... said common source region having a portion that has been implanted with said first ions,' is repetitive. Corrections are required."

Applicants note that the recitations were introduced in Applicants' 08/18/2003 amendment for the purpose of clarifying the chronology of the process sequence, in response to the 6/18/2003 Office Action But as discussed earlier, the Examiner still fails to appreciate the chronology and regarded these phrases redundant and repetitive. Applicants submit that with the amendment of the recitation, "said predefined areas having been implanted with said ion," in claim 1, it is now clear that the floating gate is formed after the common source region has been formed and has been implanted with the ions, because the floating gate has a substantial portion overlying the area which has been implanted with the ions. Similarly, in claim 14, the recitation, "'.... said common source region having a portion that has been implanted with said first ions," further clarifies that the floating gate is formed after the common source region has been formed and has been implanted with the ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed.

Therefore, claims 1 and 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Applicants request that the Examiner's objections to Claims 1 and 14 be removed.

Rejection of claims under § 103(a)

The Examiner rejected Claims 1 – 14 and 6 under 35 U.S.C. 103(a) as unpatentable over Lin et al. (US 6,355,527) in view of wht the Examiner considers admitted prior art. Applicants respectfully traverse the rejection of these claims.

To establish a *prima facie* case of obviousness under §103(a), each of three requirements must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine references or modify a reference. (MPEP § 2143.01.) Second, a reasonable expectation of success must exist that the proposed modification will work for the intended purpose. (MPEP § 2143.02.) Moreover, both of these requirements must "be found in the prior art, not in applicant's disclosure." (MPEP § 2142.) Third, the reference or references, taken alone or in combination, must disclose or suggest every element recited in the claims. (MPEP §2143.03.)

Because all the claims do not stand or fall together, Applicants will present argument for each claim groups.

Claim Group 1

The Examiner has maintained his rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI ERA: Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322). Here, the Examiner suggested that Lin et al. disclosed a method for forming split-gate flash memories with improved, increased coupling ratio and that Wolf, pp. 321 – 322, showed adjustment of channel threshold voltage using ion implantation. The Applicants disagree with the Examiner's argument.

In rejecting Claim 1, the Examiner stated in the 10/20/2003 Office Action,

"Regarding Claim 1, Lin et al. clearly disclose a method for forming split-gate flash memories with improved, increased coupling ratio. A common source region is formed (125) (Figure 2G) in a silicon substrate. Source implantation is done using n-type implants (Col. 6 lines 42 – 45) and drains (120) implanted at opposite sides of the source (and within the vicinity (second extremity) of gate regions) (Figure 2G) using n-type implants (Col 7, lines 14 – 18). Floating gates (140) (Figure 2D) are formed, overlying areas of the common source region (Figure 2D) and extremities extending over the (first) part of the structure."

It appears that the Examiner ignored the chronology in Lin's disclosure, both in the specification and claims, which forms the floating gate before the source region implant, , as discussed earlier, Also as discussed earlier, Claim 1 of the instant invention clearly demonstrate a chronology. Claim 1 now recites floating gate formation after ion implantation into the common source region , such that a substantial portion of the floating gates overlies the implanted common source region in the substrate. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. Lin fails to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions." Wolf also failed to teach these claimed process steps.

The Examiner combined Lin et al. with Wolf to teach a concept of threshold voltage implanting. The combination of these references still fails to show or suggest the elements of claim 1. Claim 1 also recites that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell, among other elements. Although Wolf could have taught a general concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed.

Accordingly, Claim 1 is patentable over the cited references.

Claim Group 2

The Examiner rejected claims 2 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

Applicants submit that dependent Claim 2 that is dependant from the amended claim 1 is also patentable. The dependent claim 2 is patentable at least for the reasons given above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 2 when combined with independent claim 1. Therefore, Claim 2 is patentable over the cited prior art.

Claim Group 3

The Examiner rejected claims 3 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

The Applicants submit that dependent claim depends from the amended claim 1, and therefore, is also patentable. The dependent claim is patentable at least for the reasons given

above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claim 3 when combined with independent claim 1. As noted, Claim 3 is also patentable for other reasons.

In particular, Claim 3 further recites that the ions implanted to form the common source region include arsenic ions. The Examiner stated in paragraph 5 on page 3 in the Final Office Action mailed October 20, 2003,

> "Although Lin et al. disclose (col. 6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can bbe readily calculated and implant conditions altered accordingly. *Since the phosphorus diffuses slightly faster than arsenic (page 68), it would be desirable to use arsenic* and therefore obvious to one of ordinary skill in the art at the time of the invention since *both would produce similar results* and thus to combine Sze, Wolf and Lin et al. to obtain ion implant n-type impurities within a flash memory device to form source regions."

Applicants note that the Examiner's statements include arguments that appear inconsistent. In the above statement, the Examiner alleged, "...Since phosphorus diffuses slightly faster than arsenic, it would be desirable to use arsenic ..". But in the "Response to Arguments" the Examiner stated, "...lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling," (paragraph 14, page 10, of the Final Office Action mailed on 10/20/2003). It would then follow that using arsenic instead of phosphorus for source implant in Lin et al. would have resulted in less lateral diffusion and would have decreased the coupling ratio. How could the Examiner state that it would be desirable to use the slower-diffusing arsenic ? The Examiner's arguments appear inconsistent.

As discussed earlier, the coupling ratio in the instant invention is determined by the patterning process which determine the overlap between the floating gate and the source. Because the instant application does not depend on lateral diffusion for increased coupling ratio, arsenic can be advantageously used to make shallow devices.

In addition, Lin et al. clearly taught away from using arsenic in source region implant. For example, Lin at al. stated (Col. 6 lines 42 – 44), "Source implant is accomplished, preferably, by using phosphorous ions." In addition, even though claim 21 of Lin et al. suggested using arsenic for drain region implantation, claim 15 of Lin et al. clearly recited using phosphorus for source region implantation. Accordingly, the combination of Lin et al., Wolf, and Sze not only failed to show or suggest, but actually taught away from, the elements of claim 3 in the instant application. Accordingly, there is no *prima facie* case of obviousness. Therefore, claim 3 is patentable over the cited references.

Claim Group 4

The Examiner rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI ERA: Vol.1 – Process Technology," Lattice Press, Sunset Beach, Ca., (1986), pp. 321 – 322).

Because Claim 4 depends from Claim 1, Applicants believe that claim 4 is allowable for at least the same reasons that claim 1 is allowable. In addition, the Examiner correctly noted that the use of sacrificial oxides is not disclosed. Here, the cited references do not show or suggest the combination of elements included in claim 4 when combined with independent claim 1. Therefore, Claim 4 is patentable over the cited prior art.

Claim Group 5

The Examiner also rejected claims 5 and 9 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 5 and 9 depend from Claim 1, Applicants believe that Claims 5 and 9 are patentable for at least the same reasons that claim 1 is patentable. In addition, Lin et al. and Wolf, taken either separately or in combination, did not disclose or suggestion, at least, " implanting ions into said first and second floating gate regions to adjust said threshold voltage;" and "wherein said ions include Boron ions." Although Wolf could have taught a generally concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed. Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Applicants believe claims 5 and 9 are patentable over the cited references.

Claim Group 6

The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

Because Claim 6 depends from Claim 1, Claim 6 is patentable for at least the same reasons that claim 1 is patentable. In addition, as the Examiner correctly pointed out Lin et al. did not explicitly identify a conductive layer. Wolf also failed to disclose or suggestion, at least, " forming a conductive layer over said second polysilicon layer;.."; " Absent a disclosure of each claim element and motivation to modify Lin et al., there is no prima facie case of obviousness. Accordingly, Claim 6 is patentable over the cited references.

Claim Group 7

The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, further in view of Mizuno ("Hot Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure," IEEE Trans. On Electron Deices, Vol. 38, No. 3, (1991), pp. 584 – 591.)

Because Claim 7 depends from Claim 6, Applicants believe that claim 6 is patentable for at least the same reasons that claim 6 is patentable. In addition, as the Examiner correctly pointed out that Lin et al. did not disclose the composition of the spacer as a nitride. Although Mizunno could have taught a generally concept of nitride spacers, it failed to show or suggest the claim elements of the method for the flash memory device described in Claim 7. Claim 7 recites, *inter alia,* "forming a nitride layer over the first oxide layer, performing an etching process to remove a portion of the nitride layer and leaving nitride spacers adjacent the side walls of each of the floating gates, and forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer,..."

The Examiner alleges that "..it would have been obvious to one of ordinary skill in the art at the time of the invention to use the nitride spacers of Mizuno et al in Lin et al. and to combine Mizuno et al. with Wolf and Lin et al. to obtain appropriate hot carrier suppression." In making this statement, the Examiner fails to realize that a flash memory device utilizes hot carrier injection for programming. Any method for hot carrier suppression would be counterproductive. The Examiner, in fact, produced a motivation to not use the claimed method. Accordingly, Applicant submit that claim 7 is patentable over the cited references.

Claim Group 8

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, and further in view of Wilson ("Handbook of Multilevel Metallization for Integrated Circuits, " Noyes Publ., Westwood, New Jersey, (1993), p. 868).

Because Claim 8 depends from Claim 6, Applicants believe that claim 8 is patentable for at least the same reasons that claim 6 is patentable. In addition, the cited references do not show or suggest the combination of elements included in claim 8 when combined with independent claim 6. Accordingly, Applicant believe that claim 8 is patentable over the cited references.

Claim Group 9

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above.

Because Claim 10 depends from Claim 6, Applicants believe that Claim 10 is patentable for at least the same reasons that claim 6 is patentable. The cited references do not show or suggest the combination of elements included in claim 10 when combined with independent claim 6. Accordingly, Applicants believe that claim 10 is patentable over the cited references.

Claim Group 11

Claim 11 is rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf and further in view of Wolf et al., as applied to Claim 4 above.

Because Claim 11 depends from Claim 4, Claim 11 is patentable for at least the same reasons that claim 4 is patentable. Appicants submit that Claim 11 is also patentable over the cited references for other reasons. Claim 11 recites a method in which implanting ions into the substrate to form the common source region includes implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV. The Examiner combined Wolf, Wolf et al. and Lin et al. to reject claim 11 as unpatentable under 35 U.S.C. 103(a). However, as noted in the previous discussion on claim 3 in Claim Group 2, the combination of Lin et al., Wolf, and Wolf et al. not only failed to show or suggest, but actually taught away from using arsenic in the source region implant as recited in claim 11 in the instant application. Accordingly, Applicants believe claim 11 is patentable over the cited references

Claim Group 12

Claims 12 and 13 are rejected under U.S.C. 103(a) as being unpatentabe over Lin et al. in view of Wolf, as applied to Claim 5 above.

Because Claims 12 and 13 depend from Claim 5, Applicants believe that claims 12 and 13 are patentable for at least the same reasons that claim 5 is patentable. In addition, Applicant believe Claims 12 and 13 are patentable for other reasons. For example, Lin et al. did not disclose at least " depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C ..." Accordingly, Claims 12 and 13 are patentable over the cited references.

Claim Group 13

Claims 14 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al.

The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory as recited in the instant application. In the Response to Arguments in the Office Action mailed October 20, 2003, the Examiner also stated that there was no chronology of process steps disclosed in the reference or recited in the claims of the instant application. As discussed earlier, Applicants respectfully submit that the claim 14 has been amended for clarification purposes and demonstrate certain chronology. Claim 14 now recites each floating gate region having a substantial portion overlying the common source region which has a portion that has been implanted with the first ions. Here, implanting ions occurs before forming the floating gates since a substantial portion of the floating gates overlies the implanted portion of

the common source region, the common source region having a portion that has been implanted with the first ions. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. As discussed earlier, Lin et al. used a completely different process sequence

Therefore, Claim 14 as amended clearly demonstrates a chronology of process sequence that is different from the process sequence described in Lin et al. Lin falis to disclose or suggest, at least, "forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said first ions"

The Examiner also combined Lin et al. with the threshold implants of Wolf, the nitride spacers of Mizuno et al., and the conductive tungsten layers of Wilson et al. to teach a flash memory cell with increased coupling ratio. Applicants assert that the combination of these references fails to show or suggest the claimed combination of elements for fabricating a flash memory device having a high coupling ratio recited in claims 14. As noted earlier, Lin et al. taught a different method of increasing the coupling ratio by using a separate polysilicon layer to provide coupling with the source region, which has nothing to do with Claim 14 of the instant invention.

With regard to threshold implant, lthough Wolf could have taught a generally concept of threshold voltage implanting, the combination of cited prior art still failed to show or suggest the method recited in Claim 14 which includes patterning and etching nitride masking layer to expose at least one first portion and at least one second portion of the first polysilicon layer overlying a portion of the implanted common source region, and implanting ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device.

Similarly, although Mizuno et al. could have taught the general concept of nitride spacers and Wilson et al. could have taught the general concept of using tungsten as a conductive layer, these references in conjunction with Lin et al. still failed to teach the combination of elements in claim 14, which includes, *inter alia,* forming second gate oxide over the first gate oxide layer, over the nitride spacers and over the floating gate oxide layer, forming a second polysilicon layer over the second gate oxide layer, forming a conductive layer over the second polysilicon layer, and removing portions of the conductive layer, second polysilicon layer, second oxide layer, nitride spacers and first gate oxide layer to form a plurality of select gates having a portion overlying a portion of an associated one of the floating gates. As noted earlier, the Examiner actually suggested that Mizuno taught using the nitride spacer to reduce hot carrier effects, whereas in a flash device, it is desirable to enhance hot carrier effects for programming. Thus the cited references teach away from the elements of the instant invention.

With these reasons and as discussed earlier, It is clear that Lin et al. and the other cited references, taken either singly or collectively, failed to show or suggest the combination of claim elements of claim 14. Accordingly, claim 14 is also patentable over the cited references.

Claim Group 14

Claims 16 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14.

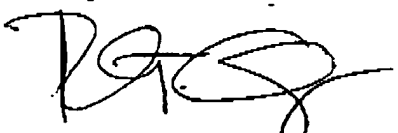
Applicants respectfully disagree. Since claim 16 is dependant from independent claim 14, Claim 16 is patentable for at least the reasons given above. Additionally, the cited references did not show or suggest the claim elements in claim 16, which recites that the first ions include N-type ions and the second ions include P-type ions. Therefore, Applicants submit that claim 16 is patentable over the cited art.

CONCLUSION:

In view of the foregoing arguments distinguishing claims 1–14 and 16 over the art of record, Applicants respectfully submit that claims 1–14 and 16 are in condition for allowance, and respectfully request that and objections to Claims 1 and 14 be removed and the rejection of Claims 1–14 and 16 be reversed.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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Encl.: Appendix of claims involved in appeal

APPENDIX – LISTING OF THE CLAIMS

1. A method of fabricating a flash memory device including an array of split gate cells, comprising:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each pair of said cells;

implanting ions into predefined areas of each said common source region;

forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming drain regions associated with said cells, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming floating gates includes the steps of:

forming a tunneling oxide layer over each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose first and second portions of said first polysilicon layer, said exposed first and second portions substantially define first and second floating gate regions;

implanting ions into said first and second floating gate regions to adjust said threshold voltage;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, said remaining portions of

said first polysilicon layer forming first and second floating gates associated with each said cell, said floating gates having side walls and a portion which overlies a portion of said common source region thereby providing a high coupling ration for the associated cell.

6. A method of fabricating a flash memory device as recited in claim 1 wherein said step of forming said select gates includes the steps of:

forming an insulating layer over the exposed portion of said substrate and the floating gate oxide layer covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form said select gates.

7. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate and said floating gate oxide layer covering said floating gates includes the steps of:

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. A method of fabricating a flash memory device as recited in claim 5, wherein said ions include Boron ions.

10. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming drain regions associated with each cell includes the steps of:

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and

11. A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region includes:

implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV.

12. A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C in order to form said first layer having a thickness in the range of 500 to 2500 angstroms.

13. A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. A method of fabricating a flash memory device having a high coupling ratio, comprising :

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions, each said floating gate region having a substantial portion thereof overlying said common source region, said common source region having a portion that has been implanted with said first ions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating ate having side walls;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer;

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates;

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least on drain area of said substrate; and

implanting third ions into said drain area of said substrate to form at least one drain region;

whereby the floating gate having a portion which overlies a portion of said common source region thereby providing a high coupling ratio for an associated cell.

15. (Cancelled)

16. A method of fabricating a flash memory device as recited in claim 14, wherein said first ions include N-type ions and said second ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted.

17 – 20. (Withdrawn)